PRESENTATION OF CCME-BASED BIDIRECTIONAL DC-DC BOOST CONVERTER WITH RECTIFIER ACTIVE BRIDGE INTEGRATION FOR CONTROL AND POWER TRANSFER AT SOURCE-TO-LOAD GATE

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Summary

The purpose of this work is to find alternatives for a DC-DC converter topology based on the TSSC (Three-State Switching Cell) that enables bidirectional power transfer between the ports connected to the converter. The integration of a transformer for coupling to the DC converter windings is used to connect an active rectifier bridge that will transfer power to a PV module, which will serve as a reference for the voltage to be implemented in the DC bus of the converter with MPPT tracking. The tests and implementations seek performance in power applications above 1 kW, checking whether such observed efficiency can be taken to high power applications.

Keywords: converter, CCTE, PV module, MPPT.

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1. Introduction

The growing need for diversification of the energy matrix, at an international level, is one of the preponderant factors of the international geopolitical scenario. Specifically in Brazil, the massive insertion of alternative energy sources has been increasingly motivated by public policies, among which the National Energy Plan 2030 (PNE) and the National Energy Efficiency Plan (PNEE) deal with the support for planning and execution of energy conservation measures (Altoé, 2017).

The works proposed in (Bascopé and Barbi, 2001) discuss the use of three-state switching cells (TSSC) in the configuration of DC-DC converters, proposing advantages of lower cost and construction volume, in addition to the reduction of conduction losses and lower current oscillations at the input and output. Thus, they are seen as possible alternatives in low voltage and high current applications, especially in powers above 1kW.

2. Presentation of the proposal topology

The presented topology is based on Jucyara (2024), and shown too in Fig. 1, a unidirectional DC-DC Boost converter based on the modified three-state switching cell (TSSC), which is magnetically coupled with a rectifier full bridge connected to a photovoltaic panel with MPPT (Maximum Power Point Tracking) control implemented. As for the Boost topology, the configuration consists of a DC voltage source, present at port 1, in series with an input inductor L_{in} two controllable bidirectional switches S_1/S_2 and two diodes D_1/D_2, and a DC bus – formed by a capacitor C_2 and its series resistance R_{c2} – interconnected to port 3.

Regarding the integration with the controlled Full-Bridge configuration, it is given by the primary windings L_1 and L_2 (adjusted by tap), and the secondary winding L_3 that constitute a high-frequency transformer. The parameters of leakage inductance, winding resistance and turns ratio define the voltage levels to be obtained at ports 2 and 3, specifically at the DC bus of capacitors C_1 and C_2. Finally, there is the set of bidirectional and controllable rectifier bridge switches $S_3/S_4/S_5/S_6$ and a DC bus – formed by capacitor C_1 and series resistance R_{c1} – connected to port 2.

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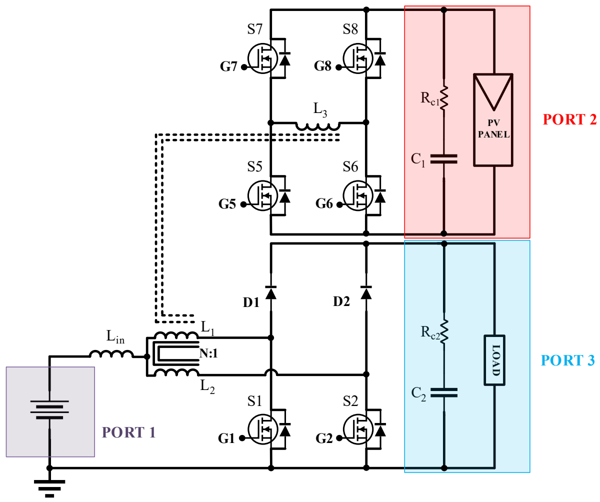

Fig. 1. Reference topology.

The boost converter in Fig. 1 allows only unidirectional flow, from the battery to the load. The idea of this work, therefore, is to propose changes to the structure that enable bidirectional flow, that is, battery recharging. The control loop implemented will be maintained and the transformer turns ratio also remains unitary. Verification of the previous and modified topologies will occur by evaluating the current flow in the semiconductors switches and the input inductor. Furthermore, the power delivered at each stage of operation will be verified, considering to evaluate the converter's efficiency.

Initially, the first modification to be made is to replace diodes D_1 and D_2 with MOSFET switches, maintaining the same parameters, such as conduction losses and trigger signal for bidirectional switches. Additionally, the control signal for the replacement switches should be revised to avoid the need for major changes to the control loop. Therefore, the topology with the modifications – and for study in this work – is presented in Fig. 3.

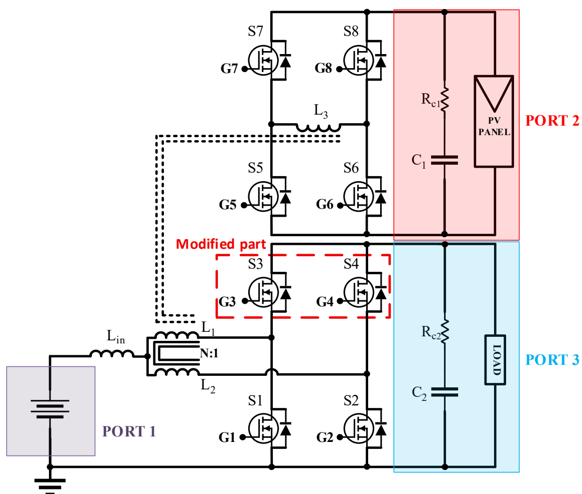

Fig. 2. Topology proposed for analysis and study

3. Proposed methodology

After the changes made to the reference topology, it is necessary to verify whether the desired objective was achieved. This verification will be based on parameters such as current flow and power between ports 1 and 3. Furthermore, some additional adjustments to the activation of the inserted switches (S_3 and S_4) will be listed to achieve the desired operation. Finally, operational aspects related to the converter's efficiency will be shown and discussed, using quantitative values and qualitative evaluations collected in computer simulations performed for the current model.

4. Operation principle for the proposed topology

The idea behind the topology, as previously stated, is to provide bidirectional power flow between the various ports integrated into the configuration. The switching period of the switches ensures overlapping current flow in the inductor loops L_1 and L_2. Therefore, each pair of 3SSC switches must operate at a different duty cycle over a period, operating simultaneously at a duty cycle greater than and less than 50%. Specifically for the purpose of this study, Boost Mode will be used with superposition conduction for switches.

Even though it's a Boost converter-based structure, the analysis for determining static gain differs from the traditional model. The switching cell allows the converter to operate in three distinct states over a switching period. The following table shows the state of each switch in the cell, noting that one of the states repeats at two points in the cycle (states 1 and 3). Fig. 3 shows the corresponding states of the topology according to the table.

Table 1: Conducting states of the switches in the switching cell of the boost converter.

States	S_1	S_2	S_3	S_4
1	ON	ON	OFF	OFF
2	ON	OFF	OFF	ON
3	ON	ON	OFF	OFF
4	OFF	ON	ON	OFF

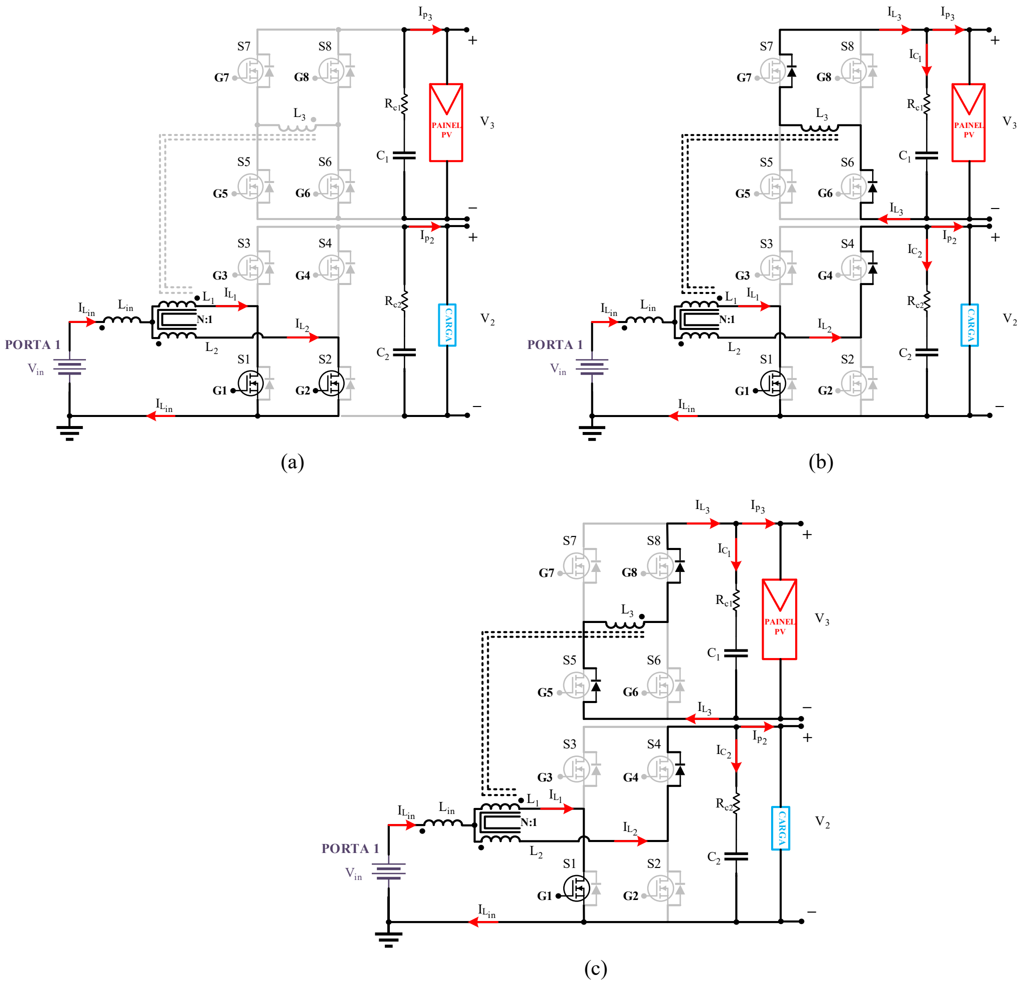

Fig. 3. Different operating states of the 3SSC Boost converter operating in Boost Mode (D≥0,5).

In this operating mode, S_1 and S_2 will be activated together with S_5 - S_8 through a control logic, while switches S_3 and S_4 will also be activated to allow conduction from their antiparallel diodes towards gate 3. Over a period of operation, both the operations will be described in intervals presented below and the waveforms shown.

First Interval ($t_0 \le t < t_1$): Switches S_1 and S_2 are activated, so that port 1 energizes L_{in} and inductors L_1 - L_2, obtaining a voltage divided equally across these inductors. Also, switches $S_5 - S_8$ remain non-energized. The photovoltaic module at port 2 supplies voltage to bus C_1, while bus C_2 powers the load (port 3). The configuration of this operating instant is shown in Fig. 3a. The inductor energization is defined by Eq. 1 given by the Kirchhoff's Law:

$$V_{L_{in}} = V_1 \rightarrow \frac{di_{L_{in}}}{dt} = \frac{V_1}{L_{in}} \text{ (for State 1)}$$

$$\therefore \frac{\Delta i_{L_{in}}}{\Delta t} = \frac{V_1}{L} \rightarrow \Delta i_{L_{in},1} = \frac{V_1(2D-1)}{2L_{in}} \quad \text{(Eq. 1)}$$

Second Interval ($t_1 \leq t < t_2$): While switch S_2 is open, switch S_4 is activated in a complementary manner, so that S_1 continues to conduct. The input inductor current L_{in} decreases linearly due to the current that now flows to the load through S_4 and winding L_2. The resulting variation in the magnetic flux, caused by the differential current in the transformer, energizes inductor L_3. Through implemented logic, switches S_6 and S_7 are activated, allowing current to flow through the antiparallel diodes to gate 3 (Fig. 3b). Since the current is divided equally between L_1 and L_2, the load voltage will be half the final value V_2. Therefore, Eq. (2) shows the decrease in the input inductor current in this interval:

$$V_{L_{in}} = V_1 - \frac{V_o}{2} \rightarrow \frac{di_{L_{in}}}{dt} = \frac{2V_1 - V_o}{2L_{in}} \text{ (for State 2)}$$

$$\therefore \frac{\Delta i_{L_{in}}}{\Delta t} = \frac{2V_1 - V_o}{2L_{in}} \rightarrow \Delta i_{L_{in},2} = \frac{(2V_1 - V_o)(1-D)T}{2L_{in}} \quad \text{(Eq. 2)}$$

Third Interval ($t_2 \leq t < t_3$): At this moment, switch S_2 switches to the conducting state, while S_1 still conducts. The pair S_3 and S_4 remain blocked, so the state is similar to that of the first interval, seen in Fig. 4a.

Fourth Interval ($t_3 \leq t < t_4$): Switch S_2 remains conducting, while S_1 is blocked. On the other hand, switch S_3 allows current flow to the load, linearly reducing the inductor current L_{in}. Thus, as in the second interval, the current flowing to the load is half the total input current. In the Full-Bridge configuration, the transformer winding L_3 has its polarity reversed and switches S_5 and S_8 are activated for flow through the antiparallel diodes (Fig. 3c). The main waveforms of the Boost operating mode are shown in Fig. 5.

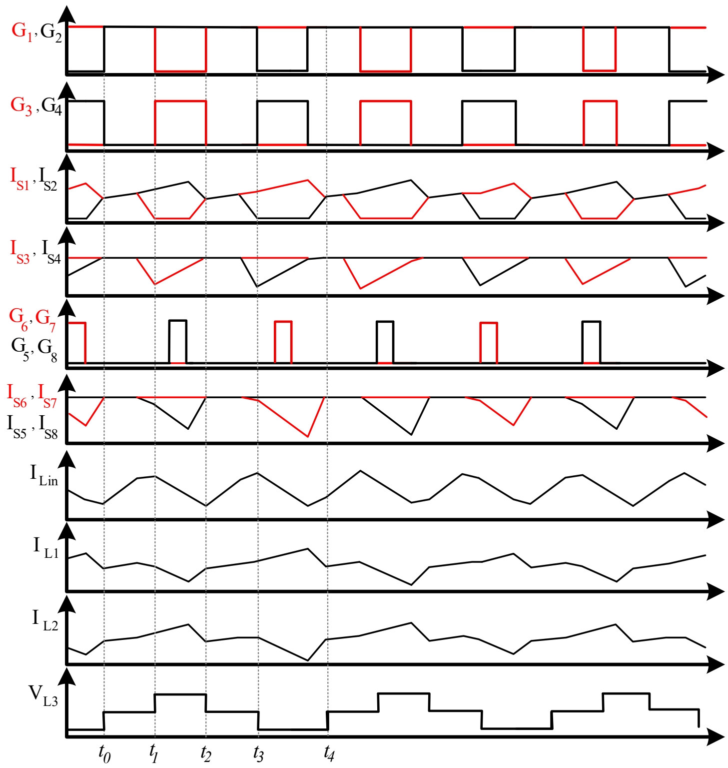

Fig. 4. Waveforms of the topology in Boost operating mode.

5. Operational modifications

Based on the work in Melo (2014) and Barrozo (2010), the control used is based on the Average Current Control strategy and is used to control the voltage supplied to ports 2 and 3. This technique consists of two loops: an internal, faster loop that controls the inductor current and an external (and slower) loop to control the output voltage. Some of the advantages are high immunity to noise, correction of sub-harmonic oscillations resulting from spikes at the time of switching and power factor correction, as demonstrated in Dixon (1999). As mentioned in Praça *et al.* (2017), power flow control occurs naturally, without the need to apply a control strategy specifically to direct this flow.

The modulation of the DC-DC converter and the Full-Bridge configuration are interdependent and require correct treatment. The converter is activated using a pulse width strategy (PWM – Pulse Width Modulation) with phase shift, in which the control signal u(t) is taken as a reference for comparison with a carrier signal. Thus, the carriers $\boldsymbol{c_1(t)}$ and $\boldsymbol{c_2(t)}$ are triangular, 180° out of phase with each other. The generated signal $\boldsymbol{d(t)}$ will activate switches $\boldsymbol{S_1}$ and $\boldsymbol{S_2}$, in such a way that the signal from switch $\boldsymbol{S_2}$ will also be 180º out of phase with switch $\boldsymbol{S_1}$. At the same time, the signals from switches $\boldsymbol{S_3}$ and $\boldsymbol{S_4}$ act in a complementary manner, respectively, to switches $\boldsymbol{S_1}$ and $\boldsymbol{S_2}$. The scheme is shown in Fig. 5.

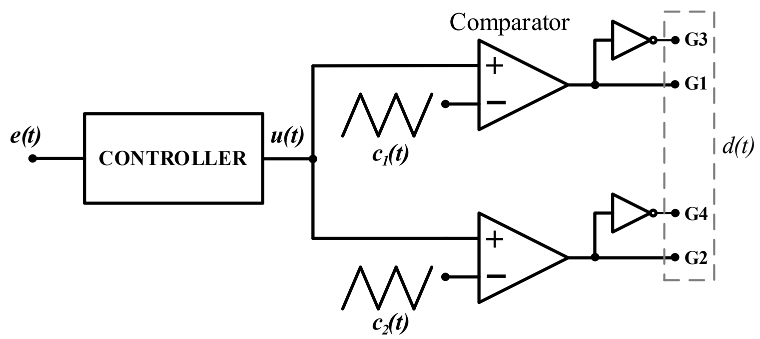

Fig. 5. Modulation to activate the DC-DC converter switches.

When switching between converter operating modes, the switching states of the main switch pairs are checked. In Boost mode, the conduction of switches $\boldsymbol{S_1}$ and $\boldsymbol{S_2}$ overlaps, justified by an operating duty cycle greater than 50%. In Buck mode, the actuated switches $\boldsymbol{S_3}$ and $\boldsymbol{S_4}$ do not conduct simultaneously, configuring the non-overlapping mode because they operate with a duty cycle complementary to that of Boost mode, i.e., less than 50%. (Fig. 6). For switches in the Full Bridge configuration, activation is defined by a logical relationship that compares:

I) A signal proportional to the duty cycle calculated for MPPT to the modules connected to port 2, u_{mppt}, presented by the works developed in (Chin *et al*., 2015; Ahmed, J., Salam, Z., 2015; Jucyara *et al*., 2024). The control signal is generated from MPPT tracking using the Perturb and Observe Adaptive Size method. The principle of this method is to compare the instantaneous current power of the module – from the current voltage and current values – and apply a defined incremental perturbation, which will generate new values of current, voltage and corresponding power. This power value will be compared with the previous value, to generate the corresponding duty cycle signal to approximate the maximum power value;

II) Triangular carries $c_1(t)$ and $c_2(t)$.

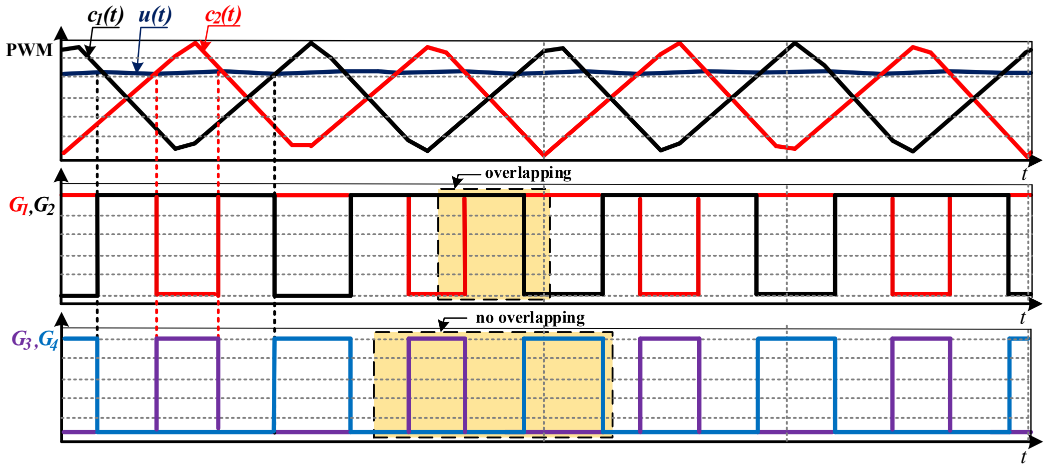

Fig. 6. Activation signals of the main switches of the DC converter operating in Buck (G_3, G_4) and Boost (G_1, G_2) mode.

However, this set of switches should only activate after the transformer windings are energized, which occurs when switches $\boldsymbol{S_1}$ and $\boldsymbol{S_2}$ overlap. From this point on, $\boldsymbol{S_5}$ and $\boldsymbol{S_8}$ are conditioned to act together during the actuation of $\boldsymbol{S_3}$ (complementary to $\boldsymbol{S_1}$), while $\boldsymbol{S_6}$ and $\boldsymbol{S_7}$ during the actuation of $\boldsymbol{S_4}$ (complementary to $\boldsymbol{S_2}$). To this end, a truth table was drawn to verify the activation of the rectifier bridge, based on the performance of the 3SSC and the considerations made. It can be seen, therefore, that the states refer to a logical AND relationship between $\boldsymbol{X_1}$ and $\boldsymbol{X_2}$ – resulting PWM between $\boldsymbol{u_{mppt}}$, $\boldsymbol{c_1(t)}$ and $\boldsymbol{c_2(t)}$, respectively – and the complementary operation of the main switches in Boost mode, $\boldsymbol{G_1}$ and $\boldsymbol{G_2}$. The activation logic circuit is shown in Fig. 7.

X_1	$\overline{G_1}$	Y_1
0	0	0
0	1	0
1	0	0
1	1	1

X_2	$\overline{G_2}$	Y_2
0	0	0
0	1	0
1	0	0
1	1	1

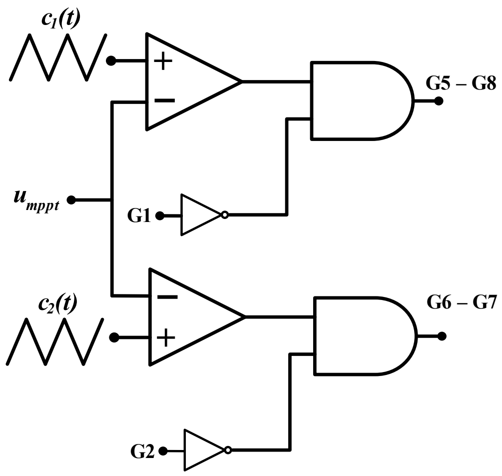

Fig. 7. Full Bridge configuration drive circuit.

6. Design specifications and results

In terms of specifications for a model for simulation and theoretical validation of the converter, Table 1 presents the listed parameters. Regarding the transformer used, Table 2 shows the values used in the simulation.

Table 2: Converter specifications.

Parameters	Value
Input voltage - Port 1 [V_{in}]	100 V
Input inductor [L_{in}]	132 µH
Equivalent series resistance of capacitor DC bus – Port 2 [R_{c2}]	0,08 mΩ
Equivalent series resistance of capacitor DC bus – Port 3 [R_{c1}]	0,08 mΩ
Capacitance of Port 2 [C_1]	470 µF
Capacitance of Port 3 [C_2]	470 µF
Output voltage – Port 2 e 3 [V_2 e V_3]	360 V
Switching frequency [f_s]	20 kHz
Test resistance – Port 2 [R_{p2}]	162 Ω
Test resistance – Porta 3 [R_{p3}]	83 Ω
Duty cycle [D]	0,72
Power Port 2 [P_{p2}]	1,5 kW
Power Port 3 [P_{p3}]	1,5 kW

Table 3: Transformer ratings.

Parameters	Value
Resistance of primary winding [R_p]	100 µΩ
Resistance of secondary winding and terciary winding refered to primary [R_s - R_t]	100 mΩ
Primary winding leakage inductance [L_p]	1 µH
Leakage inductance of secondary and tertiary windings referred to primary [L_s - L_t]	4 µH
Magnetizing inductance seen by the primary [L_m]	2 H
Number of turns of the primary winding [N_p]	40
Number of turns of the secondary winding [N_s]	20
Number of turns of the tertiary winding [N_t]	20

The parameters were taken from the Jucyara (2025) model and will be the same for the modified converter of this work, simulated in the PSIM® software. The behavior of the output voltage will be verified – the main objective being to provide a DC voltage at the output of ports 2 and 3 – as well as to evaluate whether the current flow of port 3 will change. To perform this verification, an auxiliary switching was added in conjunction with a current source at port 3 to switch the operating mode from Boost to Buck at $0.25\ s \leq t < 0.5\ s$ and $0.75\ s \leq t < 1\ s$. Fig. 8 shows the voltage and current behavior at port 3 in the two operating modes in simulation.

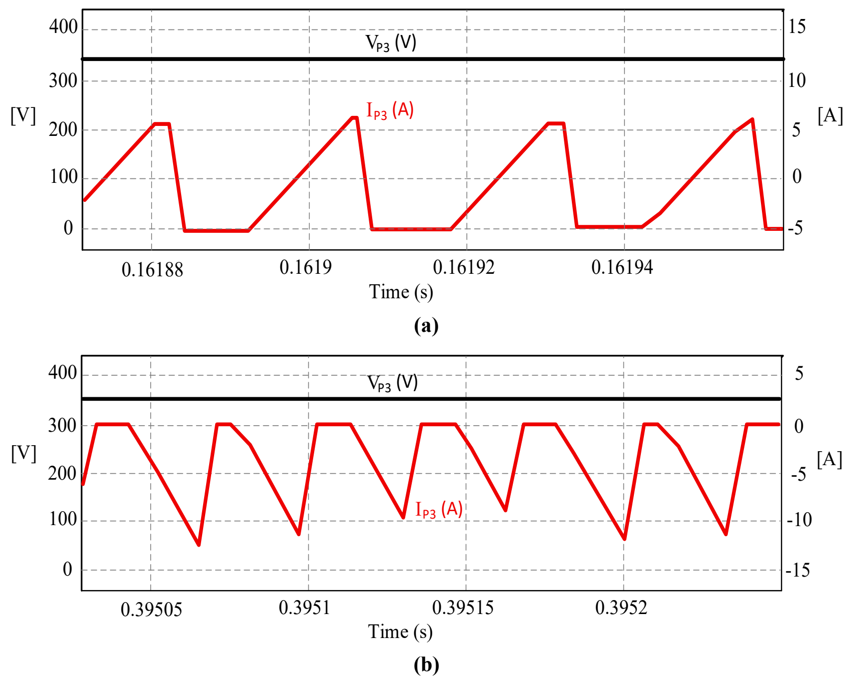

Fig. 8. Voltage and current waveforms at port 3 from the topology modified: (a) Boost mode and (b) Buck mode.

It can be seen that direction of the current in Boost mode is positive (Fig. 8a), that is, flowing to port 3. In Buck mode (Fig. 8b), the current presents an opposite flow, now supplied by port 3. The average values of the current $\boldsymbol{I_{P3}}$ for Boost and Buck modes, respectively, are 4.339 and 4.158 A. Therefore, there was a little loss of part of this current in the transformer due to the modeled winding resistances, in addition to part of this flow being transferred to port 2.

About the power flow in port 1, Fig. 9 shows the average power value at that during the transitions between the converter's operating modes. Note that at certain intervals the average value is negative, demonstrating a power flow toward the source. However, the full-bridge configuration of port 2 can also supply power, so it is more important to confirm whether the same occurs with port 3.

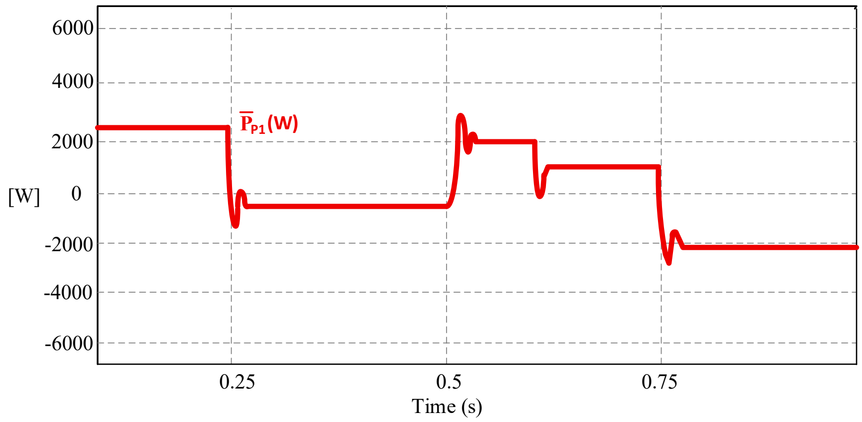

Fig. 9. Average power curve for port 1.

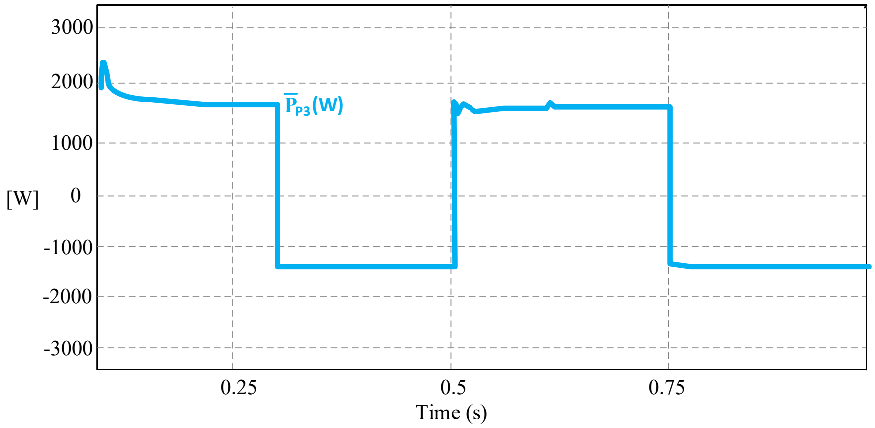

Fig. 10. Average power curve for port 3.

Therefore, the same average power verification was performed on port 3, following the same switching stages between operating modes as can be seen in Fig. 10. The power flow variation was observed, presenting a positive average value in Buck mode, resulting in an inverse transfer of the power flow to the transformer windings.

In both average power behaviors at ports 1 and 3, the control drive system responds quickly to flux changes throughout the simulation period, demonstrating that the average current method – originally implemented – is effective in controlling the current. However, losses occur due to some non-idealities considered in the simulated circuit, such as resistance and leakage inductance of the transformer windings and capacitors. Quantitative values of voltage and current stresses on the switches and other passive elements of the model are presented in Table 4, 5 and 6.

For each interval, in terms of power supplied and absorbed, it obeys the following flows:

Stage 1 ($\boldsymbol{0 \leq t < 0.25}$): Port 1 feeds Port 2 and 3

Stage 2 ($\boldsymbol{0.25 \leq t < 0.5}$): Port 3 feeds Port 1 and 2

Stage 3 ($0.5 \leq t < 0.75$): Port 1 and 2 feed Port 3

Stage 4 ($0.75 \leq t < 1$): Port 2 and 3 feed Port 1

Table 4: Quantitative values of average power (in W) and efficiency in each interval.

Parameters	Stage 1	Stage 2	Stage 3	Stage 4
Average Power $\bar{P}_{P1}$	2431.41	-709.94	944.53	-2232.7
Average Power $\bar{P}_{P2}$	799.6	793.4	-743.5	-792.6
Average Power $\bar{P}_{P3}$	1577	-1543.13	1564.05	-1543.1
Efficiency	96.3%	97.4%	92.6%	95.5%

Table 5: Quantitative values of maximum voltage effort in some components

Parameters	Value
L_{in}	100 V
L_1, L_2	180 V
S_1, S_2, S_3, S_4	360 V
S_5, S_6, S_7, S_8	360 V

Table 6: Quantitative values of average current for switches in each interval.

Parameters	Stage 1	Stage 2	Stage 3	Stage 4
Average Current $\boldsymbol{L_{in}}$	24.3 A	7.09 A	9.43 A	22.3 A
Average Current $\boldsymbol{L_1}$	12.1 A	3.66 A	5.18 A	10.6 A
Average Current $\boldsymbol{L_2}$	12.1 A	3.40 A	3.90 A	11.6 A
Average Current S_1	9.97 A	1.45 A	2.74 A	8.35 A
Average Current S_2	9.73 A	1.40 A	2.04 A	8.94 A
Average Current S_3	2.13 A	1.99 A	2.43 A	2.30 A
Average Current S_4	2.45 A	1.79 A	1.85 A	2.72 A
Average Current S_5	0.84 A	1.00 A	1.20 A	1.24 A
Average Current S_6	1.00 A	1.16 A	0.60 A	0.41 A
Average Current S_7	0.84 A	1.00 A	1.20 A	1.24 A
Average Current S_8	1.00 A	1.16 A	0.60 A	0.41 A

A tensão de saída das portas P2 e P3 é apresentada na Fig. 11. Nos dois primeiros estágios, o comportamento da tensão pelo método de rastreamento e correspondente controle possui um valor mais aproximado ao definido, alterando-se nos estágios 3 e 4 com maior erro. A Tabela 7 mostra o valor médio de tensão em cada intervalo e a taxa de erro estimada.

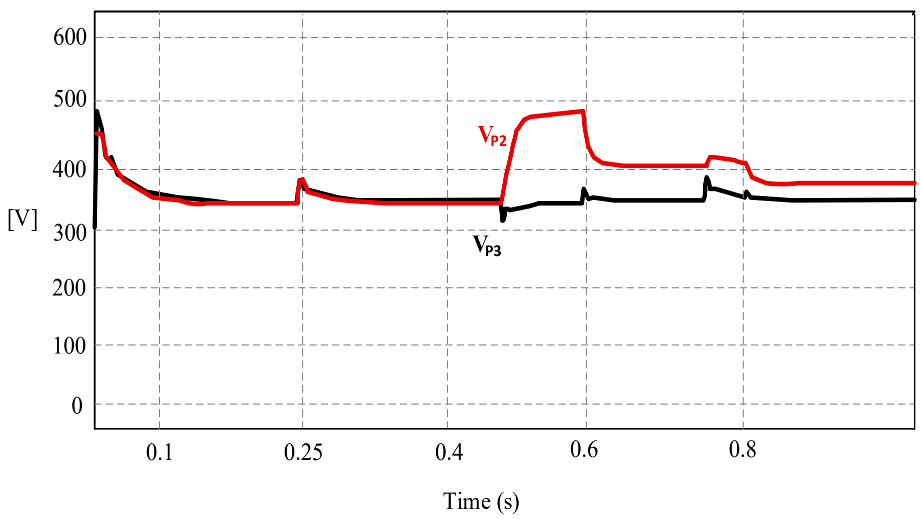

Fig. 11. Output voltage behavior for Port 2 and 3.

Table 7: Quantitative values of voltage and mean error for ports 2 and 3 in each interval.

Parameters	Stage 1	Stage 2	Stage 3	Stage 4	Mean Error $\|\epsilon - \epsilon_o\|$ %
Average Voltage V_{P2}	358.62	358.22	394.63	376.80	0.037
Average Voltage V_{P3}	360.49	360.17	360.21	360.20	0.00074

7. Conclusion

The topology proposed in this work utilizes the three-state switching cell in static converters, whose function is to adapt the power flow between the ports according to need. Through component modifications and adjustments to the drive control, the previously semi-bidirectional topology now provides bidirectionality between all connected ports, as observed in the simulated models. The efficiency verified for the average power in each distinct stage of operation shows high performance, despite not considering conduction losses in the switches and input inductor. Furthermore, the switches operate with high voltage stress, which can induce eddy currents and temperature rise during operation.

Regarding the control used, the average current control technique proved to be suitable and provided a satisfactory response for the established voltage control. Thus, operational steps were described, switch switching graphs, and relevant signal behaviors were plotted and discussed.

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